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**FEE TRANSMITTAL
for FY 2005**

Effective 10/01/2004. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT** (\$) **500.00****Complete if Known**

Application Number	09/503,939
Filing Date	February 14, 2000
First Named Inventor	GAFKEN, Andrew H.
Examiner Name	O.T. Akpati
Art Unit	2135
Attorney Docket No	2207/8478

METHOD OF PAYMENT (check all that apply)
☐ Check ☐ Credit card ☐ Money ☐ Other ☐ None
Order
☒ Deposit Account:Deposit
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11-0600

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☒ Charge fee(s) indicated below ☒ Credit any overpayments☒ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee
to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1)

(\$ N/A)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims - 30 ** = 0 X 50 = 0

Independent Claims - 5 ** = 0 X 200 =

Multiple Dependent X = 0

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203		2203		Multiple dependent claim, if not paid
1204		2204		** Reissue independent claims over original patent
1205		2205		** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2)

(\$ 0)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for <i>ex parte</i> reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

(\$ 500.00)

SUBMITTED BY**Complete (if applicable)**

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Signature

Date

February 28, 2005



AF/ 21 35 / *tlw*

PATENT
Att'y Dkt.: 2207/8478

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
GAFKEN, Andrew H.
Serial No.: 09/503,939
Filed: February 14, 2000
For: MODULAR BIOS UPDATE

Examiner: Odaiche T. Akpati

Art Unit: 2135

APPEAL BRIEF

Mail Stop Appeal Briefs - Patent

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits this appeal brief in the above-referenced application. A notice of appeal was filed on December 27, 2004.

REAL PARTY IN INTEREST

INTEL Corp. is the real party in interest for all issues related to this application. INTEL Corp. owns this patent application by virtue of an assignment recorded with the Office at reel 010711, frame 0473.

RELATED APPEALS OR INTERFERENCES

There are no other appeals or interferences related to this application.

STATUS OF CLAIMS

Claims 7-10, 16-26, and 28-36 are pending in this application. Of those pending claims, claims 7, 9-10, 16-18, and 20-25 stand rejected as being anticipated by prior art. Claims 8, 19, 26, and 28-36 stand rejected as obvious over prior art. Claims 1-6, 11-15, 27, and 37-42 were canceled. All rejections are appealed.

03/02/2005 AKELECH1 00000008 110600 09503939

01 FC:1402 500.00 DA

STATUS OF AMENDMENTS

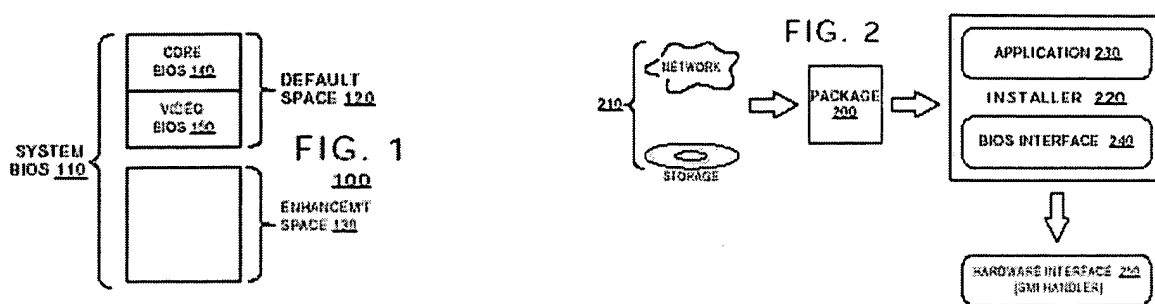
Claim 16 has been amended to correct a minor typographical error in response to the final office action. The proposed amendment was entered for purposes of appeal.

SUMMARY OF INVENTION

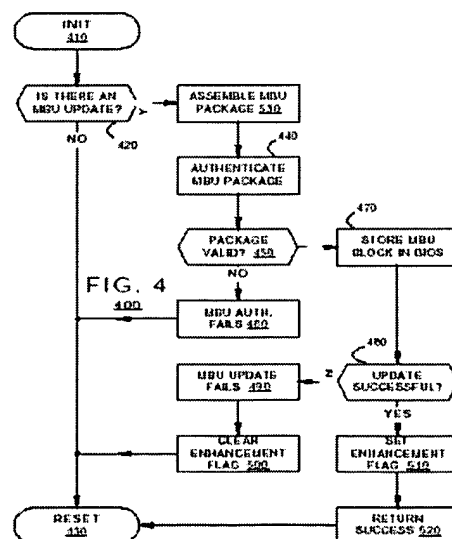
The present invention relates to BIOS management schemes for use in a computer system. Conventionally, BIOSes define input output processes for a computer system. A BIOS is executed by the computer immediately upon start up. In earlier computer systems, BIOSes were provided in ROM devices when the systems were manufactured and they could not be updated. Modern systems permit new BIOS systems to be stored in a computer system after manufacture, when the systems are in use in the field. This application contains claims directed to novel, non-obvious techniques for managing installation of BIOS updates in a computer system. Is also contains claims directed to use of the installed BIOS updates during reboot.

Installation of a New BIOS

FIG. 1 illustrates a memory space 100 storing a system BIOS 110 according to an embodiment of the present invention. The memory space 100 has a non-volatile memory space 120 and a volatile enhancement memory space 130. The non-volatile memory space 120 stores a core BIOS 140 and one or more ancillary BIOSes. These BIOSes in the non-volatile memory space 120 can not be altered after fabrication. An enhancement memory space 130 is provided, however, to store BIOS updates that supplement or replace the BIOSes stored in the non-volatile memory space 120. The enhancement memory space 130 also contains an allocation table (not shown) that maps BIOSes stored in the enhancement memory space 130 to corresponding BIOSes in the non-volatile memory space 120. Specification, pp. 2-3.



As illustrated in FIG. 2, the memory space 100 shown in FIG. 1 may be included in a computer system that receives a modular BIOS update ("MBU") package 200, a data object that has one or more BIOS packages. The MBU package 200 is input to the computer system via an input device 210. The computer system may include an installer 220 having an application program 230 and a BIOS interface driver 240 for processing the MBU package 200. The installer 220 interfaces with a computer network 210, and searches for and downloads a most recent MBU package for the computer system from the network 210. The installer 220 also validates and revises the MBU packages 200 and stores them in system memory for installation. Additionally, the installer 220 creates pointers that map elements in the non-volatile memory space 120 to those in the enhancement memory space 130. The installer sets certain flags to indicate the presence of a new MBU package in system memory and disables certain hardware security locks if necessary to prevent data writes thereto. Specification, pp. 3-4.



In operation, when located by the installer 220, the MBU package 200 is downloaded from the network 210 and stored in system memory. The computer system is then shut down without installing the BIOS update. Upon restart of the computer system, the MBU package 200 is copied to the enhancement memory space 130. FIG. 4 illustrates this operation in detail. When the system BIOS restarts, the system BIOS determines whether there is an MBU update (box 420) and authenticates the MBU package (box 440). Upon successful authentication, the system BIOS copies the MBU package to the enhancement memory space (box 470). The system BIOS then sets the enhancement flag and amends the enhancement table (box 510). Subsequently, the system BIOS may reset the entire system, which, in turn, may restart the BIOS and clear system memory (box 470). Specification, p. 6.

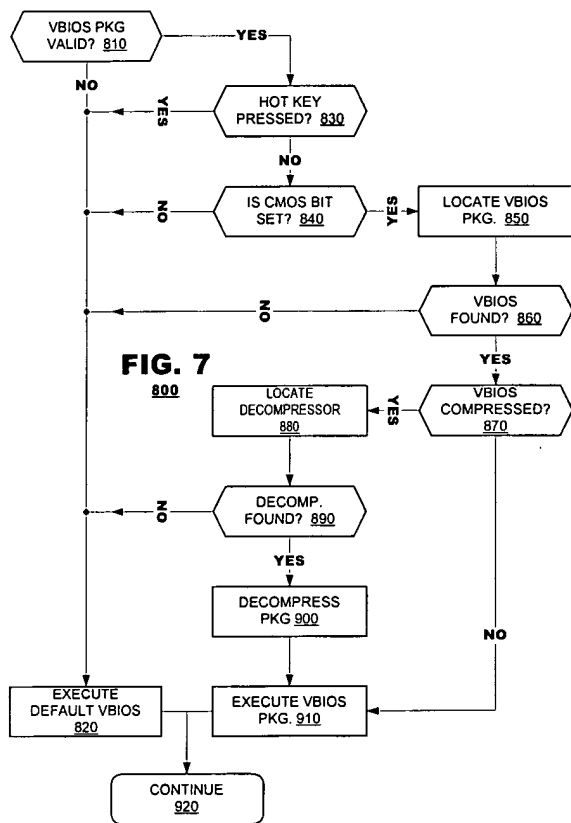
The application contains claims directed to these embodiments. Claim 7 specifies for example that, upon restart of a processor, the processor determines whether system memory contains a BIOS package, authenticates the BIOS package and, if authentication is successful, stores it in a reprogrammable BIOS memory space. None of the cited prior art teaches or suggests this method.

Boot Procedures for Computers Involving BIOS Updates

The application also presents claims directed to various techniques for selecting, from among several BIOS systems available to a processor, which BIOS will be executed. As noted, a system may store a default BIOS system, typically installed during original manufacture of a computer system, and an enhancement BIOS that is intended to replace or supplement the default BIOS.

FIG. 7 illustrates an exemplary method of executing a video BIOS package according to an embodiment of the present invention. This method illustrates several techniques that determine which of two BIOSes will be selected for use – a default BIOS 820 or the

enhancement BIOS 910. The method begins upon restart of a processor. For example, when the processor is restarted, if a predetermined hotkey is pressed (box 830), the system may execute a BIOS from the default space even if an updated BIOS is available in the enhancement space. Alternatively, the processor may check a status bit that indicates whether an updated BIOS is present in the enhancement space (box 840); if the status bit is not set, the processor may execute the BIOS from the default space rather than from an enhancement space. Specification, pp. 9-11.



These control features are recited among several of the claims, including for example, independent claims 16, 20, 22, 26, 31 and 33. None of the cited art teaches or suggest this subject matter.

Additionally, the specification explains that the default and enhancement memory spaces 120, 130 may store multiple BIOS systems. As higher levels of integration become permissible in integrated circuits, a single integrated circuit may include processing systems that formerly were distributed across multiple chips. For example, the specification describes a core

processing system and a video processing system. Each of these systems may include its own BIOS.

The present invention includes features that help manage use of multiple BIOS systems and their updates in the alterable memory system. The enhancement space includes an index table that indicates which of possibly many BIOS systems from the default space are updated by a BIOS in the enhancement space. None of the prior art discloses this feature, either.

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether the outstanding § 102 rejection to claim 7 by U.S. Patent No. 5,844,986 to Davis and the outstanding § 103 rejection to claim 8 over Davis in view of U.S. Patent No. 5,805,882 to Cooper et al. should be reversed.

2. Whether the outstanding § 102 rejections to claims 9-10 by Cooper should be reversed.

3. Whether the outstanding § 102 rejections to claims 16-18 by Cooper and the outstanding § 103 rejection to claim 19 over Cooper in view of U.S. Patent No. 6,185,696 to Noll should be reversed.

4. Whether the outstanding § 102 rejections to claims 20-21 by Noll and the outstanding § 103 rejections to claims 31-32 over Noll in view of U.S. Patent No. 6,091,430 to Bodin et al. should be reversed.

5. Whether the outstanding § 102 rejections to claims 22-25 by Noll and the outstanding § 103 rejections to claims 33-36 over Noll in view of Bodin should be reversed.

6. Whether the outstanding § 103 rejection to claim 26 in view of Bodin, the outstanding § 103 rejections to claims 28-29 over Bodin in view of Cooper, and the outstanding § 103 rejection to claim 30 over Bodin in view of Cooper and Noll should be reversed.

ARGUMENT

The anticipation rejections to claims 7, 9-10, 16-18 and 20-25 must be reversed because the cited prior art references fail to disclose each and every element of the pending claims.

Additionally, the obviousness rejections to claims 8, 19, 26, 28-29 and 30-36 must be reversed because the cited prior art references, even when taken collectively, fail to teach or suggest the subject matter of the pending claims. Because the cited art references in this application simply do not teach or suggest all claim limitations, the appealed rejections must be reversed.

Claims 7-8 Define over the Cited Art

Claims 7-8

Claim 7 stands rejected as being anticipated by Davis. Claim 8 stands rejected as obvious over Davis in view of Cooper. Claim 7 reads:

7. A method for updating a system BIOS for a processor, comprising:
upon restart of the processor, determining whether system memory contains a BIOS package,
authenticating the BIOS package, and
upon successful authentication, storing the BIOS package in a reprogrammable BIOS memory space.

The cited prior art does not teach or suggest this subject matter. Specifically, none of the cited art teaches or suggests tying a determination of whether system memory contains a BIOS Claim 7 recites specific subject matter. It recites "upon restart of the processor, determining whether system memory contains a BIOS package." Additionally, claim 7 recites "upon successful authentication, storing the BIOS package in a reprogrammable BIOS memory space." Davis fails to disclose, teach, or suggest this subject matter.

The Examiner alleges that Davis, col. 3, lines 47-54 discloses this claimed feature. This is simply not true. FIG. 3 describes Davis's BIOS modification process. In Davis, the "replace BIOS" command is generated by a BIOS management utility software running either on the host processor or on a remote system. See Davis, col. 3, lines 50-52. The new BIOS program is then stored internally. See Davis, col. 3, lines 58-60. Authentication is then performed on the local version of the new BIOS program. If the new BIOS program is valid, the previous BIOS program is deleted. If not, the new BIOS program is deleted. Thus, in Davis, the new BIOS program is stored internally before authentication is performed. Additionally, when Davis's processor restarts, there is only one BIOS program because either the previous or new BIOS program is deleted after authentication. As such, upon restart of Davis's processor, the

new BIOS program is executed without performing any check to determine whether the system memory contains a BIOS package. Accordingly, Davis does not anticipate claim 7 and the anticipation rejection to claim 7 must be overruled.

Cooper does not cure Davis's deficiency. Nothing in Cooper discloses or suggests "upon restart of the processor, determining whether system memory contains a BIOS package." Accordingly, the obviousness rejection to claim 8 must be overruled.

In view of the above, the §§ 102 and 103 rejections to claim 7 and claim 8, respectively, must be reversed.

Claims 9-10 Define over the Cited Art

Claim 9

Claim 9 stands rejected as being anticipated by Cooper. It reads:

9. A computer system, comprising:
a processor,
firmware electrically connected to the processor, the firmware comprising:
a first storage space to store a first system BIOS, the first storage space being a read only memory,
a second storage space to store a second system BIOS and an index table, the index table associating elements of the second system BIOS with elements of the first system BIOS.

Cooper does not disclose, teach, or suggest this subject matter. The Examiner erroneously alleges that the existence of an index table is inherent because Cooper discloses memory mapping. This is incorrect.

Cooper, at best, discloses RAM shadowing where a portion of the ROM BIOS is copied into the DRAM. The address of the DRAM section holding the ROM BIOS copy is then mapped onto the flash ROM address to give the same address as the ROM. Shadowing is typically performed to accelerate memory access as disclosed in Cooper. As is well known to those skilled in the art, the drawback of RAM shadowing is that the RAM set aside for shadowing cannot be used for anything else, and thus, a corresponding amount of extended memory (RAM) is lost. To reduce the memory loss, Cooper divides the RAM into three different ranges to minimize the amount of the RAM set aside for shadowing and to maximize its use. This

memory space allocation, however, does not imply that Cooper uses an index table associating elements of the second system BIOS with elements of the first system BIOS. To the contrary, an index table is not necessary because Cooper maps the ROM BIOS copy to the flash ROM to give the same address as the ROM. Neither memory shadowing nor memory mapping requires the use of an index table. Thus, it is improper to make such an inference. Accordingly, Cooper fails to anticipate claim 9.

Claim 10

Its dependent claim 10 discloses additional features that are neither disclosed nor suggested by the cited art, including:

the first storage space is to store a system BIOS, at least one ancillary BIOS, and the index table identifying the BIOSes.

Cooper does not disclose this subject matter. Nowhere in Cooper is it disclosed that the ROM stores a system BIOS, at least one ancillary BIOS, and the index table identifying the BIOSes. Thus, Cooper does not anticipate claim 10. Accordingly, the anticipation rejection to claim 10 must be overruled.

Claims 16-19 Define over the Cited Art

Claim 16

Claim 16 stands rejected as being anticipated by Cooper. Claim 19 stands rejected as obvious over Cooper in view of Noll. Claim 16 reads:

16. A BIOS processing method, comprising:
executing a system BIOS from a default memory space,
executing an ancillary BIOS according to:
 determining whether an ancillary BIOS exists in an alterable memory space,
 if no ancillary BIOS exists in the alterable memory space, executing an ancillary BIOS from the default memory space.

None of the art teaches this subject matter. The Examiner alleges that Cooper anticipates claim 16 because "with the BIOS being shadowed, this gives the operating system two areas to choose to access the BIOS." This is simply wrong. Shadowing refers to a process of copying

the contents of the flash ROM to the DRAM. The purpose of RAM shadowing is to accelerate the BIOS routine because the flash ROM has a longer access time than the DRAM. In Cooper, once the flash ROM is copied to the DRAM, the BIOS is always executed from the DRAM regardless of whether an ancillary BIOS exists. There is no need/reason to execute the BIOS from the flash ROM because the flash ROM has a longer access time than the DRAM. Thus, Cooper does not "give the operating system two areas to choose from to access the BIOS." For at least these reasons, Cooper fails to anticipate claim 16. Accordingly, the anticipation rejection to claim 16 must be overruled.

Noll does not cure Cooper's deficiency. Noll also fails to disclose, teach, or suggest executing an ancillary BIOS from the default memory space if no ancillary BIOS exists in the alterable memory space. Rather, in Noll, a copy of the BIOS always exists in both the primary and second BIOS ROMs. Noll executes a second BIOS ROM only when a data error is detected in the primary BIOS ROM. Thus, Cooper, either alone or in combination with Noll, fails to render claim 19 obvious. Accordingly, the § 103 rejection to claim 19 must be overruled.

Claims 17-18

Claims 17-18 stand rejected as being anticipated by Cooper. They recite, in part:

- if an ancillary BIOS exists in the alterable section, executing the ancillary BIOS in the alterable memory space [claim 17]; and
- determining whether a predetermined user command has been entered and, if no predetermined user command has been entered, executing the ancillary BIOS from the alterable memory space [claim 18].

The cited art do not teach this subject matter. Specifically, in Cooper, executing the ancillary BIOS in the alterable memory space does not depend on whether the ancillary BIOS exist in the alterable section. Rather, the BIOS is always executed in the DRAM after performing RAM shadowing. Additionally, nowhere in Cooper is a "predetermined user command" mentioned. The system reset disclosed in Cooper, col. 9, lines 26-20 is not a "user command" as the reset requested by the microcontroller. Thus, Cooper fails to anticipate claims 17-18. Accordingly, the anticipation rejections to claims 17-18 must be overruled.

In view of the above, the §§ 102 and 103 rejections to claims 16-19 must be reversed.

Claims 20-21 and 31-32 Define over the Cited Art

Claims 20-21

Claims 20-21 stand rejected as being anticipated by Noll. Claim 20 reads:

20. An ancillary BIOS processing method, comprising:
determining whether an ancillary BIOS package is present in an enhancement space of firmware,
if the ancillary BIOS package is present, determining whether a predetermined user command has been entered,
if the predetermined user command has not been entered, executing the ancillary BIOS package from the enhancement space,
otherwise, executing an ancillary BIOS from a default space of firmware.

Noll does not disclose, teach, or suggest the user command feature. The Examiner alleges that Noll discloses a predetermined user command because, in Noll, "if the user does not reset, the ancillary BIOS is executed, else it is not." This is simply not true. In Noll, the user does not choose whether to reset or not. Rather, when the computer has been turned on, the CPU automatically resets the error flag. Noll, col. 7, lines 3-6. The CPU then determines whether the primary BIOS ROM contains a data error. Noll, col. 7, lines 6-8. If there is no data error, the CPU executes the BIOS from the primary BIOS ROM. If there is a data error, the CPU executes the BIOS from the secondary ROM. Thus, Noll's reset flag has nothing to do with whether the BIOS is executed from the primary or secondary ROM. Accordingly, contrary to the Examiner's contention, Noll's reset flag does not represent a predetermined user command. Thus, Cooper fails to anticipate claim 20. Accordingly, the anticipation rejection to claim 20 must be withdrawn. The anticipation rejection to claim 21, which depends from independent claim 20, also must be overruled.

Claims 31-32

Claim 31-32 stand rejected as obvious over Noll in view of Bodin. Claim 30 reads:

31. A video BIOS processing method, comprising:
determining whether a video BIOS package is present in an enhancement space of firmware,
if the video BIOS package is present, determining whether a predetermined user command has been entered,

if the predetermined user command has not been entered, executing the video BIOS package from the enhancement space,
otherwise, executing a video BIOS from a default space of firmware.

As discussed above, Noll fails to disclose, teach, or suggest the user command feature. Bodin does not cure Noll's deficiency. Bodin also fails to disclose, teach, or suggest a predetermined user command or any equivalent feature thereof. Rather, Bodin discloses a high-resolution display system that simultaneously displays multiple virtual DOS applications. In displaying multiple virtual DOS application, Bodin sometimes performs a video update by writing update information to hardware via BIOS. Nothing in Bodin indicates that a predetermined user command is used. Additionally, the Examiner alleges, without citing to the references, that it would be obvious to combine the teachings of Noll and Bodin because the video BIOS and the system BIOS have analogous functionality. This assertion is unsupported because there is nothing in Noll or Bodin that provides any suggestion or motivation to combine these two references. Accordingly, the obviousness rejection to claim 31 must be withdrawn. The obviousness rejection to claim 32, which depends from independent claim 31, also must be overruled.

In view of the above, the §§ 102 and 103 rejections to claims 20-21 and 31-32, respectively, must be reversed.

Claims 22-25 and 33-36 Define over the Cited Art.

Claims 22-25

Claims 22-25 stand rejected as being anticipated by Noll. Claims 22 and 24 recite, in part:

determining whether an ancillary BIOS package is present in an enhancement space of firmware, the ancillary BIOS package including a BIOS update [claims 22, 24];

Noll does not disclose, teach, or suggest this subject matter. The Examiner alleges that Noll teaches an ancillary BIOS package including a BIOS update. This is an incorrect reading of Noll. Noll's secondary BIOS ROM contains a backup copy of the BIOS package. The backup copy, however, is the same as the BIOS package in the primary BIOS ROM. Noll, col. 3, lines 22-25. Thus, the secondary BIOS ROM does not include a "BIOS update." Moreover, Noll does not

disclose determining whether an ancillary BIOS package is present in the enhancement space of firmware. Rather, Noll always includes the BIOS package in both the primary and secondary BIOS ROMs. As such, there is no need/reason to determine whether the BIOS update is present in either the primary ROM and/or the secondary ROM. The only determination made in Noll is whether the primary BIOS ROM contains any data error. Thus, claims 22 and 24 are not anticipated by Noll. Therefore, the anticipation rejections to claims 22 and 24 must be withdrawn. The anticipation rejections to claims 23 and 25, which depend from independent claims 22 and 24, respectively, also must be overruled.

Claims 33-36

Claims 33 and 35 stand rejected as obvious over Noll in view of Bodin. They read, in part:

determining whether a video BIOS package is present in an enhancement space of firmware, the video BIOS package in the enhancement space including a BIOS update [claims 33, 35].

As discussed above, Noll does not disclose, teach, or suggest this subject matter. Bodin fails to overcome the deficiency of Noll. In particular, Bodin fails to disclose, teach, or suggest a video BIOS in the enhancement space that includes a BIOS update. Further, Bodin does not disclose determining whether a video BIOS package is present in an enhancement space of firmware. Additionally, the Examiner fails to provide any evidence of motivation or suggestion for the alleged combination. Thus, Noll, either alone or in combination with Bodin, does not render claims 33 and 35 obvious. Accordingly, the obviousness rejections to claims 33 and 35 must be withdrawn. The obviousness rejections to claims 34, and 36, which depend from independent claims 33 and 35, respectively, also must be overruled.

In view of the above, the §§ 102 and 103 rejections to claims 22-25 and 33-36, respectively, must be reversed.

Claims 26 and 28-30 Define over the Cited Art.

Claims 26, 30

Claim 26 stands rejected as obvious in view of U.S. Patent No. 6,091,430 to Bodin et al. Claim 30 stands rejected as obvious in view of Bodin over U.S. Patent No. 5,805,882 to Cooper et al. and U.S. Patent No. 6,185,696 to Noll. Claim 26 recites, in part:

during execution of a system BIOS, determining whether a video BIOS exists in an alterable firmware section of a memory system,
if no video BIOS exist in the alterable section, executing a video BIOS in a nonalterable firmware section in the memory system.

Bodin fails to disclose, teach, or suggest this subject matter. Bodin discloses a virtual device driver that supports high-resolution graphics using multiple virtual DOS applications. To support the rejection to claim 26, the Examiner relies on Bodin, col. 4, lines 41-45 and col. 5, lines 9-22 and 31-40. This citation, however, merely explains that, when the DOS application updates the display, *the system writes to the video hardware (SGVA adapter) via a BIOS if the display data includes substantial changes*. In col. 5, lines 9-22 and 31-40, Bodin then discloses in detail how the display data is written to the video hardware in two different embodiments. Bodin, however, does not disclose a memory system having a nonalterable firmware section and an alterable firmware section, let alone a nonalterable firmware section having a system BIOS and a video BIOS. Additionally, Bodin is silent on whether the display data is written to the video hardware during execution of a system BIOS. Thus, Bodin fails to render claim 26 obvious. Accordingly, the obviousness rejection to claim 26 must be withdrawn. The obviousness rejection to claim 30, which depends from independent claim 26, also must be overruled.

Claims 28-29

The dependent claims 28-29 stand rejected as obvious over Bodin in view of Cooper. These dependent claims recite other features that are neither taught nor suggested by the cited art. They recite, in part:

- if a video BIOS exists in the alterable section, executing the video BIOS in the alterable section [claim 28]; and

- determining whether a predetermined user command has been entered and, if no predetermined user command has been entered, executing a video BIOS from the alterable section [claim 29].

None of the cited art discloses this subject matter. As discussed above, Cooper does not disclose executing the video BIOS in the alterable section if the video BIOS exists in the alterable section. Additionally, nowhere in Cooper is a "predetermined user command" disclosed. Bodin also fails to disclose, teach, or suggest any of these features. Thus, Bodin, either alone or in view of Cooper, fails to render claims 28-29 obvious. Accordingly, the obviousness rejections to claims 28-29 must be overruled.

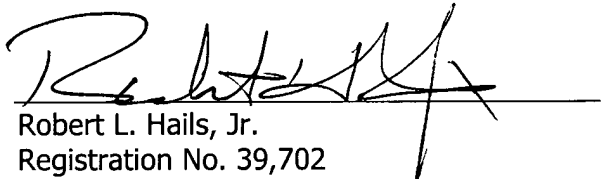
In view of the above, the § 103 rejections to claims 26 and 28-30 must be reversed.

CONCLUSION

Applicants respectfully request reversal of the anticipation rejections to claims 7, 9-10, 16-18 and 20-25, and the obviousness rejections to claims 8, 19, 26, 28-29 and 30-36. These claims are allowable over the cited art.

Respectfully submitted,

Date: February 28, 2005



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CLAIMS APPENDIX

- 1-6. (Canceled).
7. (Previously presented) A method for updating a system BIOS for a processor, comprising:
 upon restart of the processor, determining whether system memory contains a BIOS package,
 authenticating the BIOS package, and
 upon successful authentication, storing the BIOS package in a reprogrammable BIOS memory space.
8. (Previously presented) The method of claim 7, further comprising:
 determining whether the BIOS package is successfully stored in the reprogrammable BIOS memory space,
 if so, report a success flag identifying the BIOS package as successfully stored.
9. (Previously presented) A computer system, comprising:
 a processor,
 firmware electrically connected to the processor, the firmware comprising:
 a first storage space to store a first system BIOS, the first storage space being a read only memory,
 a second storage space to store a second system BIOS and an index table, the index table associating elements of the second system BIOS with elements of the first system BIOS.
10. (Original) The computer system of claim 9, wherein the first storage space is to store a system BIOS and at least one ancillary BIOS and the index table identifying the BIOSes.
- 11-15. (Canceled).
16. (Currently amended) A BIOS processing method, comprising:
 executing a system BIOS from a default memory space,
 executing an ancillary BIOS according to:
 determining whether an ancillary BIOS exists in an alterable memory space,

if no ancillary BIOS exists in the alterable memory space, executing an ancillary BIOS from the default memory space.

17. (Previously presented) The method of claim 16, further comprising, if an ancillary BIOS exists in the alterable section, executing the ancillary BIOS in the alterable memory space.

18. (Previously presented) The method of claim 16, further comprising, determining whether a predetermined user command has been entered and, if no predetermined user command has been entered, executing the ancillary BIOS from the alterable memory space.

19. (Previously presented) The method of claim 16, further comprising:
decompressing an ancillary BIOS from the alterable memory space and
executing the decompressed ancillary BIOS.

20. (Original) An ancillary BIOS processing method, comprising:
determining whether an ancillary BIOS package is present in an enhancement space of firmware,
if the ancillary BIOS package is present, determining whether a predetermined user command has been entered,
if the predetermined user command has not been entered, executing the ancillary BIOS package from the enhancement space,
otherwise, executing an ancillary BIOS from a default space of firmware.

21. (Original) The method of claim 20, further comprising:
decompressing the ancillary BIOS from the alterable section and
executing the decompressed ancillary BIOS.

22. (Previously presented) An ancillary BIOS processing method, comprising:
determining whether an ancillary BIOS package is present in an enhancement space of firmware, the ancillary BIOS package including a BIOS update,
if the ancillary BIOS package is present, determining whether a predetermined flag has been set in the firmware,
if the predetermined flag has been set, executing the ancillary BIOS package from the enhancement space,

otherwise, executing an ancillary BIOS from a default space of firmware.

23. (Original) The method of claim 22, further comprising:
decompressing an ancillary BIOS from the alterable section and
executing the decompressed ancillary BIOS.
24. (Previously presented) An ancillary BIOS processing method, comprising:
determining whether an ancillary BIOS package is present in an enhancement space of
firmware, the ancillary BIOS package including a BIOS update,
if the ancillary BIOS package is present in the enhancement space, decompressing the
ancillary BIOS package, and
executing the ancillary BIOS package.
25. (Original) The ancillary BIOS processing method of claim 24, further comprising
searching memory for a decompressor associated with the ancillary BIOS package and, if the
decompressor is not found, executing a second ancillary BIOS package from a default space of
firmware.
26. (Previously presented) A video BIOS processing method, comprising:
during execution of a system BIOS, determining whether a video BIOS exists in an
alterable firmware section of a memory system,
if no video BIOS exist in the alterable section, executing a video BIOS in a nonalterable
firmware section in the memory system.
27. (Canceled).
28. (Original) The method of claim 26, further comprising, if a video BIOS exists in the
alterable section, executing the video BIOS in the alterable section.
29. (Original) The method of claim 26, further comprising, determining whether a
predetermined user command has been entered and, if no predetermined user command has
been entered, executing a video BIOS from the alterable section.
30. (Original) The method of claim 26, further comprising:
decompressing a video BIOS from the alterable section and
executing the decompressed video BIOS.

31. (Original) A video BIOS processing method, comprising:
determining whether a video BIOS package is present in an enhancement space of firmware,
if the video BIOS package is present, determining whether a predetermined user command has been entered,
if the predetermined user command has not been entered, executing the video BIOS package from the enhancement space,
otherwise, executing a video BIOS from a default space of firmware.
32. (Previously presented) The method of claim 31, further comprising:
decompressing a video BIOS from the enhancement space and
executing the decompressed video BIOS.
33. (Previously presented) A video BIOS processing method, comprising:
during execution of a system BIOS, determining whether a video BIOS package is present in an enhancement space of firmware, the video BIOS package in the enhancement space including a BIOS update,
if the video BIOS package is present, determining whether a predetermined flag has been set in the firmware,
if the predetermined flag has been set, executing the video BIOS package from the enhancement space,
otherwise, executing a video BIOS from a default space of firmware.
34. (Previously presented) The method of claim 33, further comprising:
decompressing a video BIOS from the enhancement space and
executing the decompressed video BIOS.
35. (Previously presented) A video BIOS processing method, comprising:
during execution of a system BIOS, determining whether a video BIOS package is present in an enhancement space of firmware, the video BIOS package in the enhancement space including a BIOS update,
if the video BIOS package is present in the enhancement space, decompressing the video BIOS package, and
executing the video BIOS package.

36. (Original) The video BIOS processing method of claim 35, further comprising searching memory for a decompressor for the video BIOS package and if the decompressor is not found executing a second video BIOS package from a default space of firmware.

37-42. (Canceled).

EVIDENCE APPENDIX

No evidence is provided herein.

RELATED PROCEEDING APPENDIX

No decisions are provided herein.